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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,715	09/25/2003	David A. Luick	ROC920030293US1	6101

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IBM CORPORATION, INTELLECTUAL PROPERTY LAW
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EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,715	LUICK, DAVID A.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/10/07 have been fully considered but they are not persuasive.

Applicant argues that the Examiner's explanation is merely a statement that Dean could be modified in the manner suggested and that the Examiner fails to articulate any particular reason why the reference should be modified in the way suggested. However, although Dean's invention does not teach the use of a private cache for each processor and his invention seems to be drawn to the use of a unified cache, Dean's invention forms groups cache ways and allocates them to each processor so that each group of cache ways acts as a private cache section for that processor. Additionally, Dean also teaches that another architecture that can be implemented for a multiple processor system is one where each processor has its own private cache (Col. 2, lines 46-52), thus providing a suggestion that the a multiple processor can be employed with private caches. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Dean to implement the private cache architecture (also disclosed by Dean) since the groups of cache ways disclosed by Dean already act as independent caches and independent caches also contain cache ways. Therefore, the cache way allocation techniques of the invention could be well implemented in a private cache system. Additionally, it is well known in the art that independent caches provide for faster processor access, thus improving performance and reducing latency.

Applicant also argues that although Dean mentions private caches, it does not teach or suggest that the allocation techniques of Dean could be modified to fit private cache

architectures. However, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Dean's invention forms groups cache ways and allocates them to each processor so that each group of cache ways acts as a private cache section for that processor. Additionally, Dean also teaches that another architecture that can be implemented for a multiple processor system is one where each processor has its own private cache (Col. 2, lines 46-52), thus providing a suggestion that the a multiple processor can be employed with private caches.

Applicant also argues that the passage in Dean that mentions private caches clarifies that Dean's invention is solely directed to unified caches. Nevertheless, the fact that Dean's invention is drawn to unified caches does not mean that the same inventive concept cannot be employed in a private cache system. Dean's disclosure does not, in any way, teach away from the use of private caches. Dean simply narrows his invention to being used in unified caches. Dean recognizes that systems with private caches exists and since his cache way groups behave

as private caches, the invention could be modified to work in a private cache system particularly since private caches are known to provide faster access.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dean et al. (6,604,174).

Regarding Claim 1, Dean discloses a method for reducing latencies associated with accessing memory for more than one processors (Proc1 110 to ProcM 112, Figure 1, wherein "processes 110, 111, and 112 can be individual processors…", Col. 4, lines 15-16), each coupled with an associated cache 130, the method comprising: determining cache miss rates of the more than one processors (cache miss percentage 194, Col. 4, lines 48-58) when issuing cache requests against the caches (hit/miss indications 190 are used to determine the cache miss percentage); comparing the cache miss rates of the more than one processors (each cache miss counter for each processor in system metric 191 is compared to the others, Col. 9, lines 49-62); and allocating cache lines from more than one of the caches to a processor of the more than one processors based upon the difference between the cache miss rate for the processor and the cache miss rates of other processors ("if a processor A's miss counter is larger than processor B's miss

counter by a predetermined cache reallocation factor, some ways of the cache will be assigned to processor A", wherein cache ways comprise cache lines)

Dean's invention does not teach the use of a private cache for each processor. Instead, Dean's invention uses a single unified cache wherein groups of cache ways are allocated to each processor so that each group of cache ways acts as a private cache section for that processor. However, Dean also teaches that another architecture that can be implemented for a multiple processor system is one where each processor has its own private cache (Col. 2, lines 46-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Dean to implement the private cache architecture (also disclosed by Dean) since the groups of cache ways disclosed by Dean already act as independent caches and independent caches also contain cache ways. Therefore, the cache way allocation techniques of the invention could be well implemented in a private cache system. Additionally, it is well known in the art that independent caches provide for faster processor access, thus improving performance and reducing latency.

Claim 5 is rejected using the same rationale as that of Claim 1 wherein the threshold cache miss rate is represented by the predetermined cache reallocation factor 195 (Col. 10, lines 4-10). Additionally, in reallocating the cache ways, cache requests associated with the first processor (processor A) will be forwarded to the way that was previously owned by the second processor (reallocated way of processor B). The cache lines in the reallocated way will be replaced with those needed by processor A (see Col. 11, line 29 – Col. 12, line 7).

Claim 13 is rejected using the same rationale as that of Claim 5.

Claim 18 is rejected using the same rationale as that of Claim 5.

Claim 28 is rejected using the same rationale as that of Claim 5.

Claim 33 is rejected using the same rationale as that of Claim 5.

Claim 36 is rejected using the same rationale as that of Claim 5.

Regarding Claims 2, 14, 29, Dean discloses the method wherein determining the cache miss rates comprises counting cache misses of each of the more than one processors (hit/miss indications 190 or historical files, Col. 4, lines 24-30).

Regarding Claims 3, 15, 34, Dean discloses the method wherein allocating cache lines comprises forwarding cache requests from the processor to a private cache associated with another processor. In reallocating the cache ways, cache requests associated with the first processor (processor A) will be forwarded to the way that was previously owned by the second processor (reallocated way of processor B). The cache lines in the reallocated way will be replaced with those needed by processor A (see Col. 11, line 29 – Col. 12, line 7).

Regarding Claims 4, 16, 35, Dean discloses the method wherein allocating cache lines comprises selectively allocating cache lines based upon a priority associated with a cache request of the processor (allocation of cache ways, wherein cache ways have many cache lines, is based on the cache miss percentage wherein the processor with the highest cache miss percentage is given priority and assigned new cache ways first, Col. 10, lines 19-40).

Claims 6, 20, is rejected using the same rationale as that of Claim 2 wherein the counting of the cache misses starts as soon as the system boots (since all cache accesses are taken into account when counting the total number of misses) therefore, this must occur after a cold start and warm-up period.

Regarding Claims 7, 37, Dean discloses the method wherein comparing the cache miss rates comprises comparing the cache miss rates, the cache miss rates being associated with more than one processor modules (each cache miss counter for each processor is compared to the others, Col. 9, lines 49-62).

Regarding Claims 8, 21, 38, Dean discloses the method wherein the threshold cache miss rate predetermined cache reallocation factor is based upon an average cache miss rate for the more than one processors (see Col. 10, lines 4-10 and Col. 4, lines 48-58).

Regarding Claims 9-10, 23-24, 32, 39-41, Dean discloses the method wherein forwarding the cache request comprises selecting the second private cache based upon a least recently used cache line associated with the private caches (allocation of cache ways, wherein cache ways have many cache lines, is based on the cache miss percentage wherein the processor with the highest cache miss percentage is given priority and assigned new cache ways first, Col. 10, lines 19-40. This means that the processor with a least recently used way, due to a low cache miss percentage, gives up a cache way to allocate it to the processor with the high miss percentage).

Regarding Claims 11, 17, 25, Dean discloses the method wherein forwarding the cache request comprises selecting the cache request based upon a priority associated with the cache request (LRU algorithm preferentially writes over a process' data when that data is in a way assigned to a different process, Col. 11, lines 55-67). The LRU information 740 is representative of the least recently cache line table.

Regarding Claims 12, 22, 42, Dean discloses the method wherein forwarding the cache request is responsive to a software instruction that overrides a result of comparing the cache miss

rates to forward the cache request to the second private cache (updating of allocation way assignment performed by tag allocation controller 161, see Col. 11, lines 40-55).

Regarding Claim 19, Dean discloses the apparatus wherein the more than one processors (110-112) and the more than one private caches (Col. 2, lines 46-52) reside on more than one processor modules (see Figure 1).

Regarding Claim 26, Dean disclose the apparatus wherein the cache request forwarder (memory controller 160) inserts the cache request into a cache request queue (process to cache multiplexor 120 which holds N output addresses) for the private cache to store the memory line in the private cache (Col. 4, lines 5-23).

Regarding Claim 27, Dean discloses the apparatus wherein the cache request forwarder 160 comprises an arbitrator 161 to arbitrate between the cache request and another cache request from another processor of the more than one processor, to forward the cache request to the cache request queue (Col. 4, lines 59-65).

Regarding Claim 30, Dean discloses the system further comprising a software application to enable the cache request forwarder to forward the cache requests (updating of allocation way assignment performed by tag allocation controller 161, see Col. 11, lines 40-55) based upon the difference between the number of cache misses associated with the first processor and the number of cache misses associated with the second processor (Col. 9, lines 49-62).

Regarding Claim 31, Dean discloses the system wherein the cache request forwarder allocates cache lines of the first private cache and the second private cache based upon the difference between the cache miss rates of the first processor and the second processor (Col. 9, lines 49-62).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-TH 6:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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MR

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